ASE breaks ground 3-D packaging plant and prepare for TSV interconnects mass production

I-Micronews

ASE, the world's largest IC-packaging and test company, plans to produce ''advanced stuff'' in the plant, according to a recent article published by EETimes. This includes flip-chip and 3-D packages based on through-silicon via (TSV) technology the article report, saying further that ''It will be their TSV plant''.

ASE also has plants in China, Korea, Malaysia and elsewhere. Like many companies, ASE is seeing strong demand for its chip-packages and test services. Recently, ASE launched a cash and stock tender offer to buy all of the outstanding common shares of Universal Scientific Industrial Co. Ltd. (USI) for over $550 million.

A plethora of companies, including ASE, Elpida, IBM, Intel, Samsung, Toshiba, TSMC and others, are exploring the possibly of stacking current devices in a 3-D configuration. Experts define a true 3-D package as one that stacks various chips vertically and then connects them by deploying through-silicon vias (TSVs). The aim is to shorten the interconnections between the chips, reduce die sizes and boost device bandwidths.

So far, chip makers are shipping limited 3-D devices based on TSVs, mainly CMOS image sensors, MEMS, and, to some degree, power amplifiers.

There are several problems with TSV technology: Lack of EDA design tools; complexity of designs; integration of assembly and test; cost; and lack of standards.

SOURCE [1]

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