

Alchimer Workshop at Semicon 2010

I-Micronews

Lenix a Korean materials and equipment supplier to Samsung, Hynix and LG announced their line of fully automated modular process equipment for running the Alchimer via fill process. The system was exclusively designed for the electro-grafting and chemical-grafting processes used by Alchimer. Process modules include: isolation, barrier, Cu seed, via filling (capable to <5 micron Via Diameter) and anneal.

Alchimer CTO **Claudio Truzzi** described the latest advances in their "fully wet" TSV insulate and fill process focusing on their ability to do high aspect ratio TSV and their low COO. Alchimer technology deposits insulation, barrier and (if desired) seed using wet chemistries namely:

- Electrografting (eG) - provides wet deposition of isolation and Cu seed layers using standard plating tools. eG insensitivity to scalloping allows for up to 40µm/min etch rate, contributing to CoO reduction

- Chemical Grafting (cG) - is used to graft films on non conductive surfaces (barrier on isolation), using standard plating tools

Such wet chemistry has obvious economic advantages over dry processing such as ionized-PVD, CVD or ALD.

Alchimer chemistry is renowned for its ability to generate extremely conformal insulator and barrier seed layers in high aspect ratio vias (> 20/1) allowing smaller diameter TSV in a given thickness of silicon. This in turn means lower self capacitance and importantly lower stress, i.e when the radius is reduced 4X the stress is reduced 16X !

Truzzi compared the COO of TSV formation by iPVD and their wet chemistries using the Yole Developpement TSV+ cost model.

In addition Truzzi challenged the assumptions in the EMC-3D cost modeling and claimed that the true total cost was > \$250 per wafer vs the ~ \$165 that consortium had previously reported (shown below).

Riko Radojic of Qualcomm described how 3D gives designers more degrees of freedom. He indicated that for the next 3-5 years design flow will require the use of existing design tools. He indicated that Qualcomm can "manage the current 3D design flow using current EDA products" He thinks that current design tools will suffice until "full design suits capable of full chip reconfiguration" are available. Radojic commented that vs 2D packaging, no unique thermal issues have been found so far in 3D technology for portable applications.

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Links:

[1] <http://www.i-micronews.com/lectureArticle.asp?id=5268>