Insights from SUSS workshop on thin wafer handling at Semicon'West 2010

I-Micronews

During a panel Q&A session led by Dr. Garrou, ASE’s **Calvin Chueng** indicated that TSMC will be driving the initial use of interposers and that ASE was on board. *“We will need interposers to bond 28 nm low K die…right now it is impossible to stack such mechanically unstable materials into a stable 3D stack”* He also sees graphics chip sets needing silicon interposers because they will require solutions where the power is not channeled through the memory. Cheung also sees interposers serving as a platform for integrated passive devices (IPD) which will allow decoupling caps to get closer to where they are needed.

Bob Lanzone indicated that Amkor has backed off their focus on backside TSV fabrication which Bob feels is well under control. They are now focusing heavily on the unit operations required to handle TSV middle wafers from foundries. He says that F2F (face-to-face) CoC (chip-on-chip) technology has been qualified with Cu/Sn IMC down to 40 µm pitch. Below 40 µm he feels Amkor will move to some form of direct Cu-Cu bonding.

ITRI Deputy Div Director **Yu-Hua Chen** announced that there is now a team of > 150 professionals fully engaged in 3D design, build and test. Their goal is to have their 300 mm 3D line qualified by the 4Q 2010. The ITRI roadmap now shows CPU + RAM stacking and memory stacking in the 2011 / 2012 in lock step with Taiwanese Foundries and OSATS such as TSMC, UMC and ASE.

Wilfried Bair detailed the process module options for their XBC300 temporary bond / debond tool which is compatible with Brewer (thermal slide), 3M (laser release), HD (laser release) and TMAT (mechanical release) bond/debond processes. He announced that their bonding chambers were now stackable to allow for smaller fab footprint. Bair indicated that they have major wafer and interposer programs underway with both IMEC and ITRI.

Chris Milsincic of HD Micro described their technology to use a combination of temporary (HD 3007) and permanent (HD 7010) polyimide adhesives to avoid thin wafer handling in 3D processing. The full process flow is shown below. Laser ablation of the HD 3007 is used to remove the carrier wafer which results in a 30 sec debond time. Their throughput goal is 25 to 50 wafers/hr.

Blake Dronen of 3M described their 3D wafer support system. Their process flow which includes a laser release layer and a family of temporary adhesives which are stable from 180 to >250 C for one hour. The full process flow is shown below.

Dronen indicates that the process is in high volume production at multiple sites in Asia, Europe and the US and that installations have been qualified for 300mm TSV production by leading DRAM and Logic manufacturers.

SOURCE [1]

Links:
[1] http://www.i-micronews.com/lectureArticle.asp?id=5252