Intel on beyond 32nm CMOS and 3D TSV plans

I-Micronews

Nikkei MicroDevice: First of all, we would like to know your perspective on future technologies. When do you think the downsizing of CMOS process technologies will come to an end?

Justin: The downsizing will still continue for a long period of time. It will not stop in a short period of time like two, three or five years. So far, people who pointed out the limit of downscaling have always cited certain technological issues. For example, it is not possible to expose circuit patterns whose line width is smaller than the wavelength of light, and there is a physical limit of the thickness of a gate insulating film.

The semiconductor industry has always come up with clever solutions to such problems as technology generations regarded as limits approach. As for lithography, the solutions were OPC (optical proximity correction) and RET (resolution enhancement technique). And the solution to the issue of gate insulating film was the high-k technology.

I will give you another reason why the downscaling will not end. It is because semiconductor technologies required in the world change over time. I have a good example. It is chips for digital consumer devices and mobile phones. Their importance is rising even at Intel.

In regard to chips in this field, areas other than logic areas, such as analog, RF and input-output areas, constitute a large area on a chip. As digital consumer devices and mobile phones evolve, the area occupied by them is enlarging.

The technology generations of such peripheral areas are several generations behind in terms of downscaling compared with those of logic areas, which are core areas. So, by scaling down those peripheral areas, it will become possible to add more functions to chips. In other words, if we look at not only logic areas but entire chips, there is still room for downscaling.

If we find new applications in the future, chips suited for those applications are different from existing chips. And such a change creates room for scaling down chips.

Nikkei MicroDevice: Could you tell us about the technology to three-dimensionally stack semiconductor chips like TSV (through silicon via)?

Justin: Even now, it is better to use three-dimensional stacking for functions that are difficult to be integrated with silicon chips. For example, to integrate power amplifier circuits made with III-V semiconductors with low costs, it is better to integrate chips or wafers with one another than to integrate the circuits on silicon

chips.

From now on, three-dimensional stacking technologies will evolve in different ways. They are the TSV technology, which Intel has long been developing, a technology to bond wafers together and a method of introducing a laminated structure in the transistor process. Along with downscaling, these three-dimensional stacking technologies will lead the evolution of chips.

SOURCE [1]

Source URL (retrieved on *12/20/2013 - 7:27am*):
http://www.mdtmag.com/news/2010/08/intel-beyond-32nm-cmos-and-3d-tsv-plans?qt-most_popular=0

Links:
[1] http://www.i-micronews.com/lectureArticle.asp?id=5380