

Why Betting on 3D?

I-Micronews

What's changed, though, is the resistance by other companies to the progression of Moore's Law. There is no longer a sense of resignation that they won't be partaking in the benefits of advanced nodes. In a 3D stacked die world, it doesn't matter if the digital portion of the chip—particularly the memory and some of the logic and IP—are developed at 15nm or even 6nm. As long as the analog and some of the IP don't have to follow the same process node progression, then it no longer matters. The rest is an integration exercise, and much of chip development these days is integration, anyway.

This is a fundamental shift for the industry as a whole, and it will require some significant planning at the system level. While it's still possible to account for hot spots and signal integrity in a two-die structure, it becomes harder with each new layer. Place-and-route models have to include thermal dynamics, and they have to be built for multiple generations in the future so logic doesn't sit on top of logic and cook the chip into oblivion. This can all done with some foresight and standardized approaches, of course. It's what engineers are good at.

It also means more standardized interconnect models, most likely a network on chip type of approach, and better understanding of through-silicon vias and their effect on communication within the chip once they begin shrinking at future nodes. But what's particularly interesting is that suddenly it brings everyone that abandoned Moore's Law at 180nm back into the race. That means they will have no choice but to re-enter the market for advanced tools for everything from modeling to verification and software prototyping, and from layout to design for manufacturing.

Stacking die, for all its technological evolutionary roots, is a market discontinuity. And at every discontinuity in the industry there has been a scramble for market share, new tools and new customers. Let the race begin!

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