Qualcomm defines format for 3-D chip stress

I-Micronews

Qualcomm has already gotten support from at least one foundry and one chip assembler for the so-called Stress Exchange Format.

"*We think industry needs to get together on this, everyone needs this enablement—we'll compete on other things,*" said **Mark Nakamoto**, a Qualcomm engineer who described the technique in a paper at the Custom Integrated Circuits Conference here. The new technique is one of many efforts driving 3-D chip stacks using through silicon vias (TSVs).

The Global Semiconductor Alliance announced this week it is forming a working group on TSVs. Nokia said it has TSVs on its road map at a recent Sematech meeting in Taiwan. And Jedec is defining a standard for memory chips using TSVs. Digital cameras already use TSVs with 30-50 micron spacing to stack CMOS imagers, memories and DSPs. A range of other applications are in the labs using TSVs with spacings in the single digits, said Nakamoto. "*You will see products in the market next year,*" he said.

SEF is essentially a way existing global an local packaging models can share stress data with new local models for chips using TSVs. The 3-D stacks face stress from a variety of mechanical and thermal sources, in part because the stacked dice and vias are sometimes made of different materials. SEF calculates an overall factor called residual stress based on the result of a variety of stress factors. It applies a 3-D matrix to the silicon area and defines residual strain vectors for each sector. The approach requires foundries to supply chip designers with 3-D Process Design Kits that provide data about the materials they use. Synopsys has become the first EDA company to automate the process of porting SEF data into a tool, in this case its Fammos technical CAD program.

Qualcomm has created multiple proof-of-concept designs using SEF including some fabricated chips about which it would not share details. Ultimately, Qualcomm hopes all foundries, packaging houses and EDA vendors will support SEF. The technique "*seems to be working fairly well,*" said **Nakamoto** in an interview with EE Times at CICC. "*But right now a lot of calibration and verification cases need to be run to check that everyone on same page with these PDKs, models and tools,*" he added

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[1] http://www.i-micronews.com/lectureArticle.asp?id=5510