IBM and TSMC Discuss 3D IS vs Scaling(2)

I-Micronews

Iyer confirmed the industry consensus opinion that *"..a combination of voltage supply reduction, power budget constraints and design IP migration suggest that the days of dramatic raw performance gains from scaling are over*" and that "*...scaling, strain engineering, and improved materials (eg. Hi K) although continuing to improve performance , will do so at diminishing rates and certainly with diminishing returns*".

Iyer pointed to the integration of large amounts of low latency memory as one of the biggest challenges for modern multi-core processor design. Since modern processors contain 60-70% embedded memory, taking that memory off chip and using TSV to make such stacked memory low latency and high bandwidth can in fact cut the size of the processor chip by as much as 50%.
Iyer labeled TSV's as "..a necessary evil" which "..mess up logic or memory designs". He adds that the TSV designs need to be done efficiently and adds that "..today we can do this with about a 5% penalty on the DRAM" .

Likewise **Douglas Yu**, indicated that with the rapid cost increases being imposed by scaling TSMC sees a migration into "system scaling" of which 3D with TSV will play a major part. Yu sees copper TSV and vias middle becoming the industry standards . When questioned about their commercial commitment to silicon interposers Yu responded " Yes we will offer commercial silicon interposers as we have recently announced with our customer [Xilinx].

SOURCE [1]

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