JEDEC announces first 3D-IC standards development

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JEDEC Solid State Technology Association, the global leader in standards development for the microelectronics industry, today announced a broad spectrum of ongoing standards development work related to 3D-ICs. As the dominant provider of free and open standards for high volume semiconductor applications including device, package, reliability and test standards, JEDEC is uniquely well-positioned to develop the standards needed to move this game-changing technology into high volume product applications. 3D is particularly suited for combinations of memory with other memory or logic, and since JEDEC has led the development of functional, interface and packaging standards for several generations of semiconductor memory including DRAM, FLASH and SRAM, it has the expertise to enable 3D standards for stacked devices and mixed technology ICs. "*JEDEC standards will allow high volume products to take advantage of this exciting technology*," said **Subu Iyer**, IBM Fellow responsible for 3D integration at IBM.
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[1] http://www.i-micronews.com/lectureArticle.asp?id=6632