

## **STATS ChipPAC expands Through Silicon Via capabilities with mid-end processing**

I-Micronews

STATS ChipPAC Ltd. (“STATS ChipPAC” or the “Company” – SGX-ST: STATSchP), a leading semiconductor test and advanced packaging service provider, today announced it is expanding its 300mm Through Silicon Via (TSV) offering with the addition of mid-end manufacturing capabilities.

TSV is an important developing technology that utilises short vertical interconnections through a silicon wafer to achieve greater space efficiencies and higher interconnect densities than wire bonding and flip chip stacking. When combined with microbump bonding and advanced flip chip technology, TSV technology enables a higher level of functional integration and performance in a smaller form factor. As a longstanding leader in 3D packaging, STATS ChipPAC was one of the first Outsourced Semiconductor Assembly and Test (OSAT) providers to invest in TSV technology with a 51,000 square foot research and development facility dedicated to the development of next generation wafer level integration with TSV technology.

One of the first implementations of TSV technology is in the form of silicon interposers used to bridge 2D silicon designs into more advanced and efficient 3D configurations. Often referred to as the 2.5D technology, TSV interposers are an immediate and practical approach to die level integration using the capabilities of TSV technology. TSV interposers provide flexibility for the integration of die from different technology nodes and deliver advantages in miniaturisation, thermal performance and fine line/width spacing in a semiconductor package.

*“The driving demand behind 3D integration is the need to scale semiconductor devices to smaller and smaller geometries with higher input/output (I/O) requirements. STATS ChipPAC is enabling advancements in 3D packaging with the development and qualification of key technologies that support TSV solutions,”* said **Dr. Han Byung Joon**, Executive Vice President and Chief Technology Officer, STATS ChipPAC. *“We have had the capability to fabricate, assemble and test TSV interposers for four years and believe the timing is right to invest in 300mm mid-end TSV manufacturing for our customers.”*

STATS ChipPAC has complete front to back-end manufacturing capabilities for 200mm wafers and currently handles both chip-to-chip and chip-to-wafer assembly for TSV technology. This includes high density microbump capabilities in both solder and copper column materials, microbump bonding down to 40um pitch, thin wafer handling, wafer level underfill, thin wafer dicing and microbumps for flip chip interconnection. Microbump technology is critical to delivering fine pitch, low profile solutions for high performance devices.

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The latest TSV investment that STATS ChipPAC has made is the addition of a 300mm “mid-end” process flow that occurs between the wafer fabrication and back-end assembly process. Mid-end processes support the advanced manufacturing requirements of 2.5D and 3D TSV as well as wafer level packaging, flip chip and embedded die technology.

Dr. Han continued, “*Flip chip and wafer level packaging are important drivers of mid-end processing in addition to the anticipated growth in 3D solutions utilising TSV technology, particularly with the integration of memory and logic devices at advanced technology nodes. The initial markets that are expected to embrace 2.5D and 3D TSV technology are mobile applications and high performance processors for the computing segment. STATS ChipPAC will continue to invest and innovate in TSV technology to offer the next generation of 3D packages to our customers.*”

### **About STATS ChipPAC Ltd.**

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