Semprius ? Massively parallel pick and place: a closer look(2)

I-Micronews

Standard “pick-and-place” tools using vacuum collets are not well suited for handling devices smaller than 100µm (Semprius calls these “chiplets”) or devices thinner than ~ 20 µm. Modern “pick-and-place” tools operate at very high speeds to achieve reasonable process throughput (> 10,000 placements per hour), but this comes at the expense of placement accuracy.

“Transfer printing” is a new technique, first developed in Professor John Rogers’ group at the University of Illinois, that enables the massively parallel assembly of high performance semiconductor devices onto virtually any substrate material. This technology is being commercialized by Semprius Inc in Durham NC.

In transfer printing, an elastomeric stamp is used to selectively pick-up devices from a source wafer and then prints (places) the devices onto the target substrate. The key enabling technology is the ability to tune the adhesion between an elastomeric stamp and the semiconductor devices. The process is massively parallel because the stamp can be designed to transfer thousands of discrete devices in a single pick-up and print operation. For instance if 240 um sq chips are laid out on a wafer at 250 um pitch and they need to be placed onto a new surface at 2 mm pitch then the stamp will be made up so that the stubs on the stamp (see transfer print stamp below) are at 2 mm pitch and therefore pick up chiplets 1, 8, 16 etc. off the wafer and then come back for chiplets 2, 9, 17 etc.

The devices to be transfer printed must first go through a process to delineate and release them from their source wafer. This method utilizes the ability to release devices using sacrificial release layers underneath the device layer. In the case of silicon devices, silicon-on-insulator (SOI) wafers represent a convenient and readily available source wafer. Circuits are fabricated, using a commercially available SOI CMOS foundry process with a 5 um device silicon layer and a 1 um BOx.

Following the foundry CMOS process, a trench is cut down to the device silicon around the periphery of the device (No metal wiring levels are present in the trench area). An encapsulation layer is then applied to the SOI CMOS source wafer to protect the ILD and wiring levels during the subsequent BOx etch. The SOI CMOS wafer goes through the etch process to remove the BOx underneath the devices with HF. The devices are now completely free from the handle wafer, but held is place using tethers in the device layer. The tethers are designed to break or cleave in a controlled manner during transfer printing. Following the sacrificial etch process the encapsulating layer is removed at which points the ICs are ready for transfer-printing.

SOURCE [1]

Source URL (retrieved on *08/04/2015 - 10:21pm*):
http://www.mdtmag.com/news/2011/06/semprius-massively-parallel-pick-and-place-closer-look2

Links:
[1] http://www.i-micronews.com/lectureArticle.asp?id=7146