

Single Chip Is a Synchronous Clock Solution for SETS

The economical STC5270 is an integrated single chip solution for the synchronous clock in SDH, SONET, and synchronous Ethernet network elements. The device is fully compliant with ITU-G.813 and Telcordia GR1244 and GR253. The STC5270 accepts two reference inputs and generates two independent synchronized output clocks. Reference input frequencies are automatically detected. All reference switches are hitless. Synchronized outputs may be programmed for a wide variety of SONET and SDH as well as Synchronous Ethernet frequencies. The clock generator includes a DPLL (digital phase-locked loop), which may operate in the Freerun, Synchronized, and Holdover modes. A standard SPI bus provides access to the STC5270's internal control and status registers. The device operates with an external 20 MHz OCXO or TCXO as its MCLK.

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